Quantum C100, a Wafer Scale CMOS Detector Optimised for 100 keV Cryo-Electron Microscopy

Nicola Guerrini[1], Mohamed El Sharkawy[2], Ben Marsh[1], Jonathan Barnard[3], Matthew Hart[1], Craig Macwaters[1], Roger Goldsbrough[2], Angus Kirkland[3], Liam O'Ryan[2], Herman Larsen[1], Iain Sedgwick[1], Sam W. Hutchings[1]

[1] Science and Technology Facilities Council, Rutherford Appleton Laboratory, OX11 0QX, Didcot, UK – Tel 0044 1235 446212, email: nicola.guerrini@stfc.ac.uk

[2] Quantum Detectors Ltd, Rutherford Appleton Laboratory, OX11 0QX, Didcot, UK

[3] Rosalind Franklin Institute, Rutherford Appleton Laboratory, OX11 0QX, Didcot, UK

Abstract

Wafer scale CMOS image sensors are no longer a rarity, thanks to the adoption and the improvement of stitched manufacturing techniques. In this paper, in fact, we do not intend to focus on the sensor area, which is dictated by the application needs. What we want to showcase are the sensor performance relatively to the technology node used and its importance in the field the sensor has been designed for, cryo-electron microscopy (cryo-EM) at 100keV.

Introduction

The success of CMOS image sensors for scientific applications like cryo-electron microscopy (cryo-EM) is demonstrated by the exponential growth of the cryo-EM field in the past years and confirmed by the number of entries in the world Protein Database System.

Cryo-EM requires complex and expensive machines, especially when performed at 300keV, which can represent a limit to further expansion of the field. Recent publications[1] suggest that beam induced sample damage depends on the accelerating voltage of the microscope. This means that reducing the operating voltage from 300keV to 100keV reduces sample damage and simultaneously allows for 25% more structural information[1]. But optimal performance at 100keV require a sensor optimised for such lower energy.

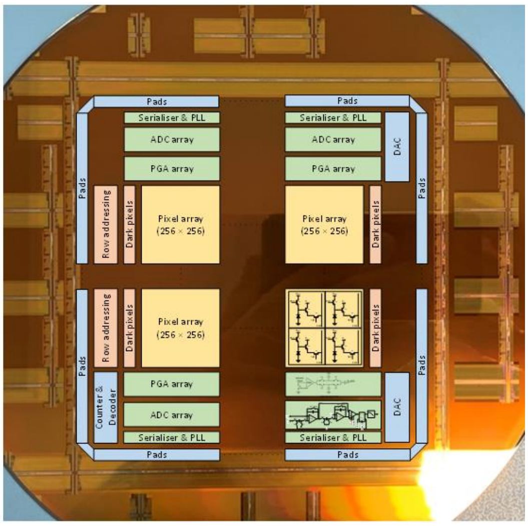

Figure 1 – C100 sensor floor plan

Specification	Target	
Sensor format	2048 x 2048	
Pixel pitch	54 x 54 µm	
Frame rate	2000 fps	2500 fps
Bit depth	12 bits	10 bits
Noise	52e- to 89e- rms, depending on gain	
Full Well	6.1ke- to 30 ke-, depending on gain	
Operation mode	Rolling shutter	
Readout mode	Continuous	
Readout type	Analogue CML lines	
Sensor size	200 mm wafer-scale sensor	
Manufacturing process	TowerJazz 180 nm CIS process	
Sensitive area	104 cm^2	
Radiation hard	YES	
Back-thinning	NO	
Dark pixels	Only on left and right sides of the pixel array	

Figure 2 – C100 performance table

Optimal detection of 100keV electrons mean larger pixels and non-thinned sensors compared to 300keV. Thanks to the widespread availability of techniques like stitching, manufacturing wafer scale sensors on 8” or 12” platform is no longer limited to niche, low volumes applications[2,3].

In this paper we present Quantum C100, a wafer-scale CMOS imager with a gapless array of 2048 x 2048 3T pixels and 54um pitch, giving a total detection area of 10.6 x 10.6cm. The uninterrupted large detecting area is one of the main advantages of CMOS image technology over other solutions for cryo-EM.

Sensor architecture

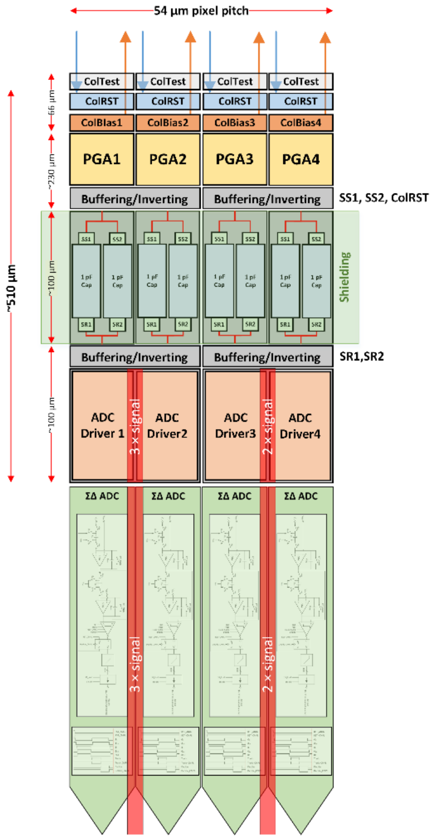

Figure 3 – C100 Column architecture

Quantum C100 is based on a rad-hard 3T pixel with rolling shutter readout and digital output. The relatively high frame rate has been achieved by reading out 8 rows at the same time.

As shown in Figures 1 and 3, rows are read from the top and the bottom of the sensor. Each 54 µm column contains 4 ADCs per side and two routing channels, to avoid signal cross-talk.

Avoiding the stacking of readout blocks minimise the signals routed over other blocks and allow for better separation of the metal tracks, key factor in maximising the manufacturing yield.

The analogue pixel value is digitised on-chip using 16,384 second order, column parallel sigma-delta ADCs. Such ADC has been chosen for it resilience over large mismatch-induced spread of the analogue stages[4].

Data transfer is achieved over 34 high-speed channels, fully compatible with the XILINX AURORA© communication protocol. This allows for greater flexibility and easier integration in the camera system.

At full resolution the sensor achieves frame rates of 2,000 to 2,500fps with a 10 or 12 bit pixel depth, but can be operated up to 5,200fps changing the bit depth.

Results

The performance of the wafer scale sensor are in line with simulated values and with the results obtained from a previous test structure. Thanks to a digitally programmable stage the gain be varied from 16 µV/e- and 90 µV/e-. Measured noise ranges from 52 e- rms to 89 e- rms depending on gain.

Full well with lower gain is ~30 ke- while it drops to 6.1ke- with the highest gain.

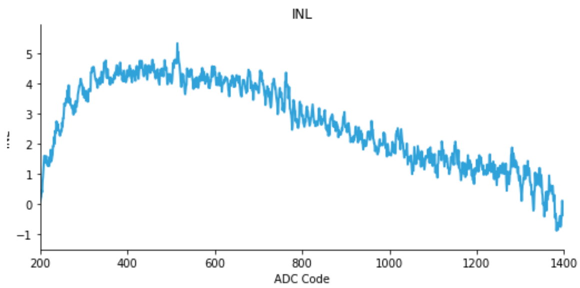

Figure 4 – Typical ADC INL

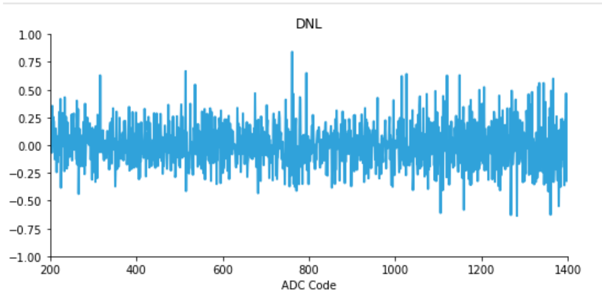

Figure 5 – Typical ADC DNL

The column parallel ADCs have been also characterised, measuring the INL and DNL performance. In figure 4 and 5 we can see the typical INL and DNL plot for a single ADC. Process variations and mismatch will obviously result in a spread of the INL and DNL performance across such large device, spread that has been minimised thanks to careful layout and component matching.

In figure 4 we can wee that the INL range is ~6ADU, from -1 to +5. In figure 5 the DNL range is ~ 1.25ADU, from -0.5 to +0.75. The INL and DNL ranges have been plotted for all 16,384 ADC in the sensor and the resulting distributions are reported in figure 6 and 7.

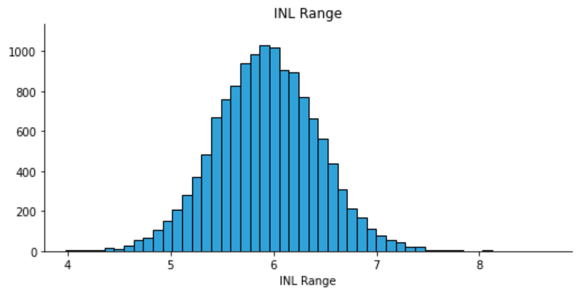

Figure 6 – ADC INL Range Distribution

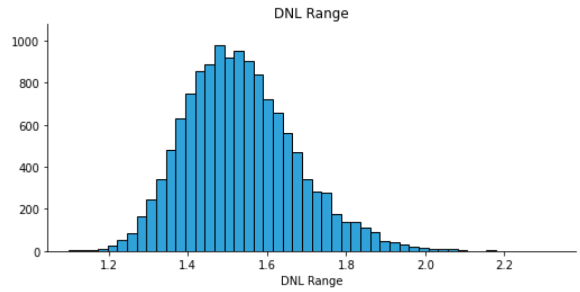

Figure 7 – ADC DNL Range Distribution

The choice of a Sigma-Delta ADC, together with the careful layout and attention to matching has clearly resulted in a very limited spread of the column parallel ADC across the entire, wafer-scale sensor.

Figure 8 – Electron microscope set-up

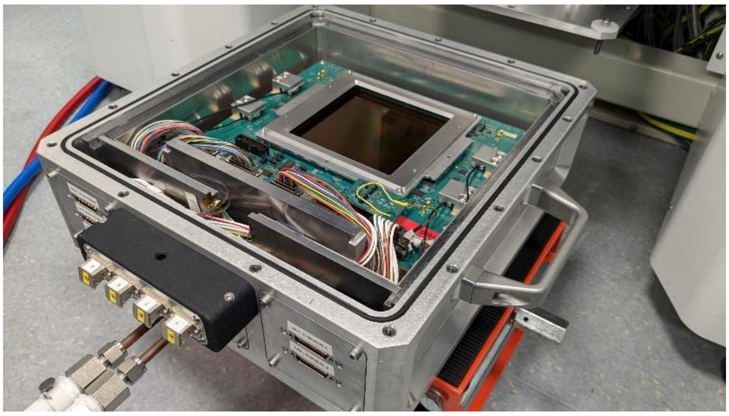

Figure 9 – Quantum C100 vacuum housing

The wafer scale sensor has been tested in a JEOL-1400 electron microscope (see figure 8) and a suitable housing (see figure 9).

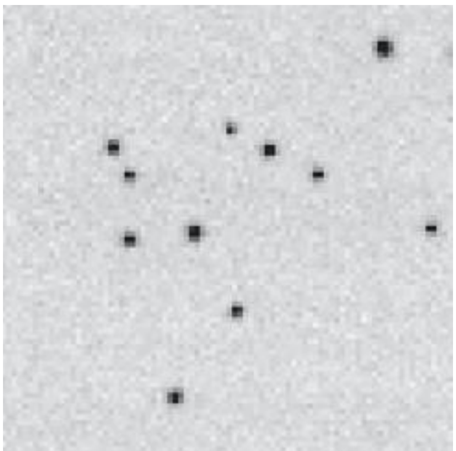

Figure 10 – 100keV electrons single events

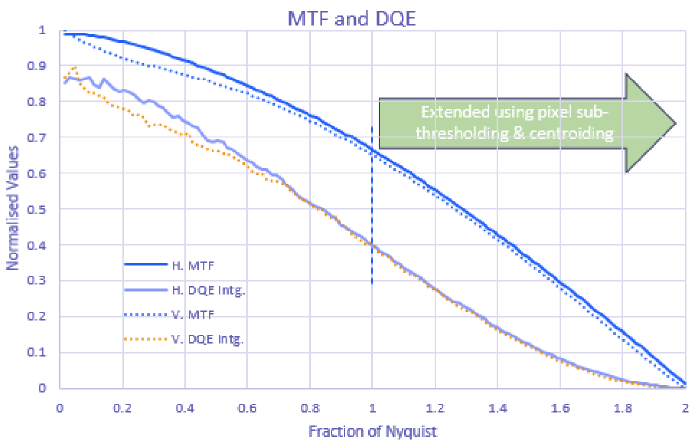

Figure 11 – MTF and DQE

Quantum C100 is optimised for the detection of 100keV electrons. Such particles deposit a relatively large signal in silicon as electrons who deposit all the energy in silicon will generate a corresponding charge of ~27.7ke-. Such charge will be spread over more than 1 pixel (see figure 10), but even a large event, that covers 3x3 pixels will see an average charge per pixel of ~3ke-, which will still give a respectable SNR between 33 and 57. Horizontal and vertical (MTF Modulated Transfer Function) and DQE (Detective Quantum Efficiency) have been measured and are reported in figure 11, confirming the excellent performance of the Quantum C100 sensor.

In figure 12 we have an image acquired with light, while in figure 13 the image has been acquired using 100keV electrons.

Figure 12 – Rosalind Franklin Picture taken with C100 sensor

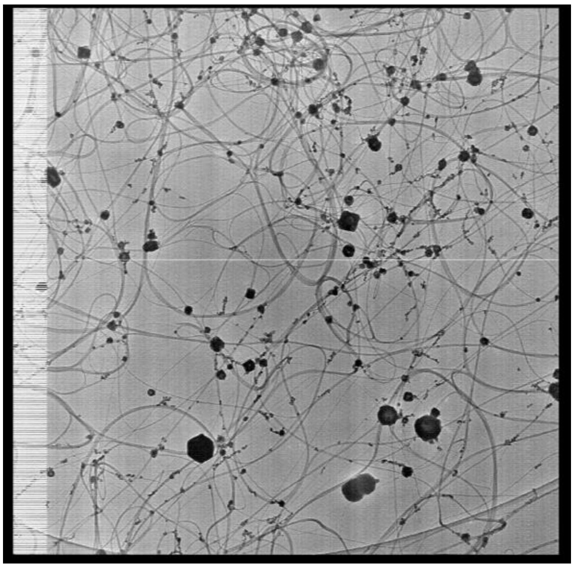

Figure 13 – Carbon nanotubes image taken with C100 in a 100keV electron microscope

The sensor output data rate is ~100Gb/s. Handling such rate with LVDS lines will present integration challenges, which we have overcome by designing high speed output stages (up to 5Gb/s). Quantum C100 is equipped with 34 high speed output lines, operating at 4.3Gb/s with a XILINX AURORA© protocol[5].

Conclusions

We have presented Quantum C100, wafer scale CMOS image sensor optimised for cryo-electron microscopy at 100keV. The measured DQE and MTF proves the excellent performance of C100, which will go into production in the second half for 2025.

References

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(5) I. Sedgwick et al., 'PRECISE: A 5Gbps Serialiser for Scientific Detectors in a 180nm CMOS Image Sensor Process', Proceedings of NSS-MIC 2022, doi: 10.1109/NSS/MIC44845.2022.10399290